A Heterogeneous Computer Architecture Accelerating Reinforcement Learning-based Design for Silicon Photonic Devices

1st Miaoxiang Yu, 2nd Zhenyu Xu, 3rd Jillian Cai, 4th Qing Yang, and 5th Tao Wei
Electrical, Computer and Biomedical Engineering
University of Rhode Island
Kingston, US
{miaoxiang_yu, zhenyu_xu, jillian_cai, qyang, tao_wei}@uri.edu

***Abstract*—This paper proposes a framework to substantially accelerate Reinforcement Learning (RL)-based design method for Photonic Integrated Circuit (PIC) devices. PICs are widely anticipated to underpin the forthcoming generation of semiconductor chips. However, the complexity of PIC design, which includes hundreds of degrees of freedom (DOF), presents considerable challenges. Machine Learning (ML) techniques, inclusive of RL, have demonstrated their effectiveness in the domain of PIC design. The primary hurdle, however, is the extended training duration, primarily constrained by the sluggish electromagnetic (EM) solver, specifically, the Finite-Difference Time-Domain (FDTD) solver. We have engineered a novel computational architecture that can be deployed on cloud-based systems using a cluster of Central Processing Units (CPUs), Field-Programmable Gate Arrays (FPGAs), and Graphics Processing Units (GPUs). An FPGA-FDTD accelerator, which capitalizes on the high memory bandwidth of on-chip memory (OCM), has been specifically designed to simulate planar PIC devices. Each FPGA-FDTD accelerator, also denoted as an FPGA kernel, functions as an autonomous RL environment. The host machine, in conjunction with the FPGA kernel, is designated as a worker node within the cluster. A functional prototype has been successfully implemented on the Amazon Web Services (AWS) cloud. The framework has effectively designed numerous PIC devices, and experimental results show the architecture outperforms existing methods significantly in design speed while maintaining or exceeding their design quality. Notably, the framework's versatility requires minimal adjustments for a broad range of devices, significantly reducing design time and promising to expedite PIC innovation.**

***Index Terms*—Silicon photonic devices, Finite Difference Time Domain, Machine Learning, Cloud Computing**

I. Introduction

Silicon photonics, in synergy with CMOS process, allows large-scale, low-cost production of integrated photonic devices. The unique functions of silicon photonic devices are due to their geometry design, optimized using various methods, including Machine Learning (ML) algorithms. However, these methods require significant time for design and optimization. Electromagnetic (EM) solvers present a critical limiting factor due to their computational intensity and the challenge of parallelizing them. To overcome this, we propose a cloud-based heterogeneous computing architecture to expedite RL-based silicon photonic device design. This involves a parallel computing cluster encompassing cloud CPUs, FPGAs, and GPUs, with a specially designed FPGA-based FDTD simulation accelerator. The architecture has been successfully implemented on AWS, significantly outperforming existing methods in terms of speed and design quality.

II. Implementation

This section will initially delve into the design of the interface between the host computer and the FPGA, as well as the deployment of the RL algorithm, as discussed in section II-A. And later, it will expound upon the formation of the RL cluster as elaborated in section II-B.

A. Hardware-software co-design

The overall architecture of the proposed RL-based silicon photonic design method is shown in Fig. 2. The software and hardware communicate via an interface module on host machine. This module takes an "action," i.e., picking a pixel in the array to change from Si-filled to air-filled. Then, it generates the corresponding pattern in the FDTD grid, i.e., the $M \times N$ data pack array. This data pack array is then downloaded to the URAM in the FPGA kernel via Xilinx Runtime Library (XRT). Sometimes, more than one type of FDTD kernel (Transverse Magnetic, TM, and Transverse Electric, TE, modes) may be required in one training step. The interface module is also responsible for observing the output (waveforms from multiple signal monitors) of the FDTD simulation accelerator, extracting the power of the field quantities of multiple signal monitors, and computing the reward.

B. Heterogeneous computing cluster for fast silicon photonic design

A cloud-based heterogeneous computing cluster is built to substantially accelerate RL-based design for silicon photonic devices, shown in Fig. 3. A cluster is formed, including CPUs, FPGAs, and GPUs. The RL training algorithm is deployed in the head node. Multiple worker nodes are connected to the head node. Each worker node contains a CPU and at

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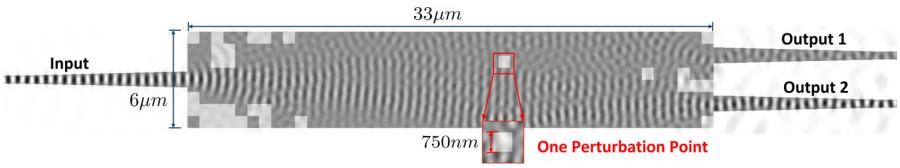

Fig. 1. Schematic of an MMI 1×2 power splitter topology with a splitting ratio of 10/90

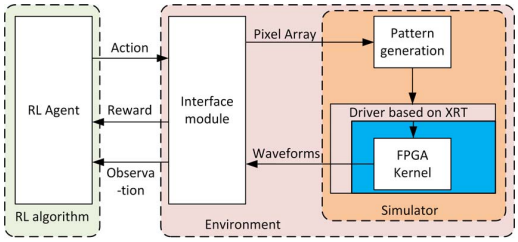

Fig. 2. Architecture of the RL-based design method

least one FPGA board attached to it. The RL agent (DNN or policy) is not trained in the worker node. The head node distributes the updated policy (DNN weights) to all worker nodes. Then, each worker interacts with the RL environment (FPGA-FDTD accelerator) and uploads the observations and rewards to the head node. The head node then collects a batch of samples (each sample corresponds to a training step) from all the worker nodes and updates the DNN (RL agent or policy). The benefit of using multiple workers is that the computationally intensive FDTD simulations are performed efficiently in parallel. Conceptually, the RL algorithm plays multiple "board games" simultaneously, making it faster to obtain an optimized design.

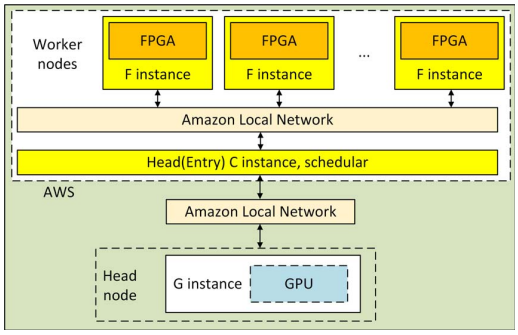

Fig. 3. Block diagram illustrating the heterogeneous computing cluster for fast silicon photonic design

III. Experiments

In this section, we present various examples of silicon photonic designs, illustrating the effectiveness and adaptability of our proposed framework. An exemplar design of a multi-mode interference 1×2 power splitter, encompassing a series of splitting ratios and configured in a 400 column by 2048 row setting within an FPGA, is depicted in Fig. 1. We conducted a speed comparison with a widely utilized commercial software optimized for parallel computation on multi-core processors. The FDTD simulation speed recorded was 50 Gcell/s. Remarkably, the proposed FPGA-FDTD accelerator outperformed the Lumerical solver by a factor of 350.0 with 1 vCPU (approximating 120 Mcell/s) and by a factor of 32.14 with 128 vCPU (1.32Gcell/s). A design of an ultra-compact polarization beam splitter is exhibited in Fig. 4.

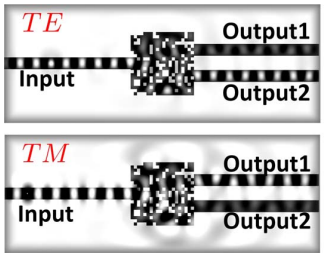

Fig. 4. Design result of the ultra-compact polarization beam splitter

IV. Conclusion

We propose a cloud-based heterogeneous computing architecture to substantially accelerate RL-based silicon photonic design. An FPGA-FDTD accelerator, leveraging the high memory bandwidth of OCM, is tailored to simulate planar silicon photonic devices. Each FPGA-FDTD accelerator, also referred to as an FPGA kernel, serves as an independent RL environment. The host machine, together with the FPGA kernel, is referred to as a worker node in the cluster. A CPU serves as the head node. The RL algorithm is deployed on the head node. The head node collects samples for a series of worker nodes in parallel, trains the DNN (RL agent or RL policy) in a GPU/CPU, and distributes the updated weights to all worker nodes to continue the RL training. Experimental results show that the proposed computing architecture is substantially faster than existing methods with comparable or better design quality. Within the scope of our study, we have established that the maximal grid size is $M \times N = 2000 \times 750$ on the target FPGA chip (Xilinx Virtex Ultrascale+ VU9P), spanning over 3 Super Logic Regions (SLRs), with a simulation speed of 112 Gcell/s. This work holds the potential to increase the pace of silicon photonic innovation significantly.

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